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Docket No.: 241944US2S

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 10/647,242
Applicant: Takehiro HASEGAWA
Filing Date: August 26, 2003
For: SEMICONDUCTOR MEMORY DEVICE INCLUDING MOS TRANSISTORS EACH HAVING A FLOATING GATE AND A CONTROL GATE
Group Art Unit: 2827
Examiner: MAI, S.
Date Allowed: May 9, 2005

SIR:

Attached hereto for filing are the following papers:

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Our check in the amount of **$0.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time.

Respectfully submitted,

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Docket No.: 241944US2S

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:	:
Takehiro HASEGAWA	: EXAMINER: MAI, S.
SERIAL NO: 10/647,242	: DATE ALLOWED: May 9, 2005
FILED: August 26, 2003	: GROUP ART UNIT: 2827
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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

The following comment is in response to the Statement of Reasons for Allowance provided in the Notice of Allowability dated May 9, 2005.

The Statement of Reasons For Allowance included on page 2 of the Notice of Allowability states that the claims are allowable because the prior art fails to teach or reasonably suggest a semiconductor memory device having various specific features. The Applicant submits that this statement does not describe the claimed subject matter recited in allowed independent Claims 1 and 14 of the present application.

In order to clarify the record, the Applicant notes that Claim 1 expressly recites:

> 1. A semiconductor memory device comprising: a plurality of memory cells each of which includes a first MOS transistor with a charge accumulation layer and a control gate and a second MOS transistor having one end of its current path connected to one

> end of a current path of the first MOS transistor; a memory cell array which has the memory cells arranged in a matrix in such a manner that the memory cells adjoining in the column direction share the other ends of the current paths of the first MOS transistors or the other ends of the current paths of the second MOS transistors; bit lines each of which connects commonly the other ends of the current paths of the first MOS transistors of the memory cells in the same column; word lines each of which is formed by connecting commonly the control gates of the first MOS transistors of the memory cells in the same row; select gate lines each of which is formed by connecting commonly the gates of the second MOS transistors of the memory cells in the same row; a column decoder which selects any one of the bit lines; a first row decoder which selects any one of the word lines; a second row decoder which selects any one of the select gate lines; and first metal wiring layers which are provided for every select gate lines, each of which is formed in the row direction so as to pass through almost the central part of the memory cells, is connected electrically to the corresponding one of the select gate lines, and transmits a row select signal for the second row decoder to select the select gate line.

Furthermore, Claim 14 of the present application expressly recites:

> 14. A semiconductor memory device comprising: a plurality of memory cells each of which includes a first MOS transistor which includes a charge accumulation layer and a control gate; a memory cell array which has the memory cells arranged in a matrix; bit lines each of which connects commonly the drain regions of the first MOS transistors of the memory cells in the same column; word lines each of which is formed by connecting commonly the control gates of the first MOS transistors of the memory cells in the same row; a source line which electrically connects commonly the source regions of the memory cells and which includes a first wiring region electrically connecting the source regions of the first MOS transistors of the memory cells in the same row commonly and a second wiring region connecting the first wiring regions in the column direction; a column decoder which selects any one of the bit lines; and a first row decoder which selects any one of the word lines.

It is noted that Claims 1 and 14 recite only the features set forth above, and no additional features should be presumed or implied to be recited therein. The Statement of Reasons for Allowance does not accurately reflect the subject matter recited in Claims 1 and 14. For example, Claim 1 does not recite a floating gate MOS transistor or a select MOS transistor, as suggested by the statement. Additionally, Claim 14 does not recite a floating gate MOS transistor, a select MOS transistor and the features described as being related thereto, first metal wiring layers and the features described as being related thereto, or a row select signal for a second row decoder, as suggested by the statement. Thus, the Applicant submits that the Statement of Reasons for Allowance is not applicable to Claims 1 and 14.

Respectfully Submitted,

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